Communications

Aligned Horizontal Silica Nanochannels by Oxidative Self-Sealing of Patterned Silicon Wafers

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Arrays of aligned horizontal nanochannels located on silicon wafers are of considerable interest for various applications in the fields of nanofluidics, nanobiotechnology, and analytics.[1−4] Common fabrication procedures for such components involve the fabrication of nanogroove arrays by means of electron beam lithography, laser interference lithography (LIL), or focused ion beam techniques. Additional bonding[5−9] or deposition[10,11] steps, which are costly and technologically demanding, convert the grooves into channels. As a result, a new interface might form inside the walls of the channels, which may alter device properties and may be susceptible to mechanical failure.

Here, we report on a simple and reliable procedure that circumvents these drawbacks and allows producing horizontal (in-plane) nanochannel arrays with high spatial precision and high throughput at low costs. It is based on the self-sealing of nanogrooves in silicon wafers upon thermal oxidation. Thermal oxidation of silicon is one of the most important procedures in silicon technology. According to the classical Deal−Grove model,[12] oxidants such as molecular oxygen (dry oxidation) and water (wet oxidation) diffuse through an existing oxide layer to react with the silicon at the Si/SiO_2 interface. Temperature-dependent parameters that determine the overall growth rate of the silicon oxide include the diffusivity and the solid solubility of the oxidants within the oxide, as well as the surface reaction rate at the Si/SiO_2 interface. The volume per Si atom increases by 125% upon conversion of Si into SiO_2.[13] The oxidation of Si is therefore associated with a corresponding expansion in volume.

The presence of both convex and concave curvatures on patterned Si substrates results in a pronounced retardation of the oxide growth with respect to planar oxidation.[13−18] Therefore, the thickness of the generated SiO_2 layer is significantly smaller at corners as compared to smooth areas. The retardation effect occurs under both dry and wet oxidation conditions, but it is more pronounced at concave corners than at convex corners.[13] Kao et al. attribute the lower growth rates at corners to viscous stress in the oxide layers associated with nonuniform mechanical deformation.[15] In planar systems, only stress components parallel to the Si/SiO_2 interface exist in the newly formed SiO_2 layer, caused by the expansion in volume during the oxidation of the Si. However, in curved systems, stress normal to the Si/SiO_2 interface also occurs and counteracts the growth of the oxide layer. The oxide is pushed outward as new oxide forms at the Si/SiO_2 interface. It is stretched in convex systems, but compressed in concave systems. Because oxidants can more easily diffuse through stretched systems than through compressed systems, the retardation of the oxide growth appears to be stronger in concave structures.[15] The dependence of the oxidation rates on the curvature dominates the oxidation of nanostructures of Si with sizes below 100 nm.[16,17] Thermal oxidative self-sealing occurs independent of specific crystal orientations and should be applicable to both single-crystalline and polycrystalline Si substrates.

Figure 1 outlines the fabrication of arrays of horizontal nanochannels by oxidative self-sealing of grooves in an (110)-oriented silicon wafer covered by a 25 nm thick thermal SiO_2 layer, which had been patterned by LIL. For this purpose, we deposited a 70 nm thick antireflection layer (WiDE-8B, i-line wet developable ARC, Brewer Science, United States) and a 180 nm thick photoresist layer (TSMR-iNO27, OHKA, Japan) onto the wafer by spin-coating and generated the line pattern with HeCd lasers ($\lambda = 325$ nm).[19−22] We applied O_2 plasma (descum process) at 100 W,

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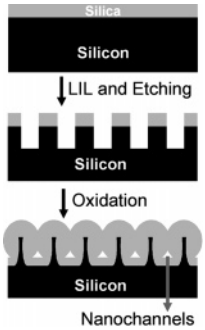

Figure 1. Schematic diagram of the fabrication of aligned, horizontal nanochannels in a (110)-oriented Si wafer containing nanogrooves by oxidative self-sealing of the grooves. Because of the retardation of the oxide growth upon thermal oxidation at the concave corners, hollow nanochannels are still present at the bottom of the grooves, whereas above the bottoms, the oxide layers growing from the opposite walls of the grooves impinge. The light gray areas denote SiO_2, the black areas Si.

30 sccm, and 10 mbar for 30 s using a S1-100 reactive ion etching (RIE) machine (Sentech, Germany) to remove residual photoresist from the developed areas. Subsequently, we removed the SiO_2 from the developed areas by RIE with CHF_3 gas plasma (100 W, 20 sccm, and 10 mbar), thus uncovering the underlying Si substrate. We then etched the grooves with 40 wt % aqueous KOH solution at room temperature. Under these conditions, the (110) faces of Si exhibit the highest etching rate.[23] As a result, an array of aligned grooves with nearly rectangular cross-sections forms. The developed areas, where no SiO_2 layer protects the Si from the base, define the position of the grooves, whereas the areas still covered by SiO_2 define the position of the walls between adjacent grooves. We removed the SiO_2 covering the nondeveloped areas by 5 wt % aqueous HF solution and oxidized the (110) wafers thus patterned in air at temperatures from 950 to 1050 °C. At the concave corners at the bottom of the grooves, the growth of the oxide is significantly retarded. Therefore, the oxide layers growing from the opposite walls of the grooves will impinge above the bottoms, whereas hollow channels are still present at the bottoms (Figure 1). Because the retardation also occurs at the convex corners at the top of the walls, the oxidized wafers possess trenches at their surface that are parallel to the channels underneath. The lithographic pre-patterning determines their position and orientation.

A representative cross-sectional scanning electron microscopy (SEM) image of an (110) silicon wafer containing aligned grooves with a center-to-center distance of 270 nm and a depth of 230 nm prior to thermal oxidation is seen in Figure 2a. The thickness of the groove walls amounted to ~130 nm. We performed the SEM investigations with JEOL JSM 6300 and 6340 scanning electron microscopes operated at an accelerating voltage of 5 kV. Self-sealing occurs if the samples are annealed at 1000 °C for 6 h. To investigate the morphology of the oxidized wafers in detail, we prepared

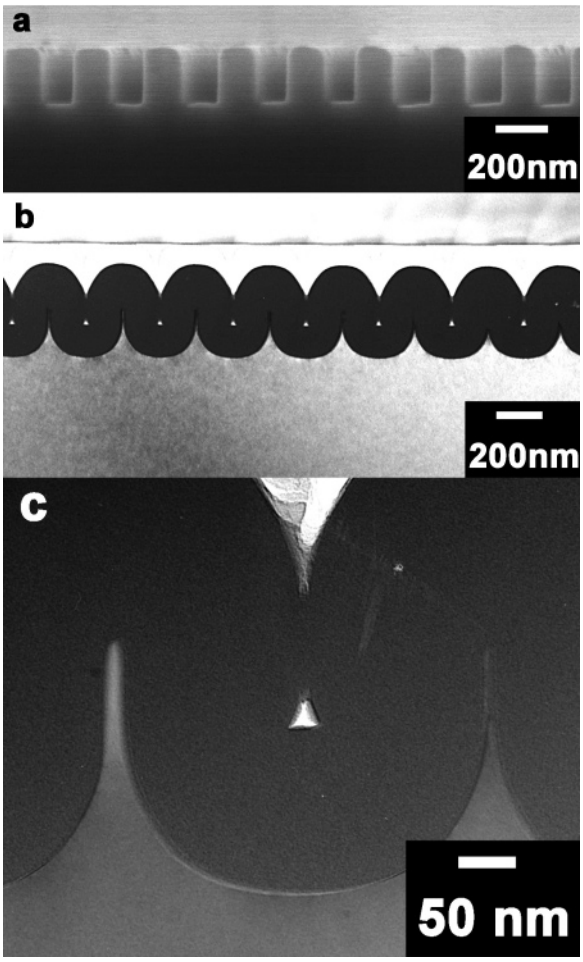

Figure 2. Oxidative self-sealing of nanogrooves in an (110)-oriented Si wafer. (a) SEM image of a cross-section of the wafer prior to oxidative self-sealing. (b,c) TEM images of a cross-sectional specimen of the wafer after the oxidative self-sealing of the grooves at 1000 °C for 6 h. The light gray areas are the Si substrate, whereas the SiO_2 layer appears in dark contrast. The nanochannels are the bright spots in the SiO_2 layer; (b) overview; (c) detail.

cross-sectional specimens for transmission electron microscopy (TEM) as follows: Two pieces of the sample were glued face to face with epoxy resin and sliced with a diamond wire saw into ~400 μm thick sections. The sections were ground and polished to a thickness of ~80 μm, upturned, dimple-ground, and further polished to a thickness less than 15 μm. The samples were then thinned to electron transparency by ion-milling from both sides with Ar (PIPS, Gatan). TEM was performed using a JEM 1010 microscope operated at 100 kV. Figure 2b shows a TEM image of a cross-sectional specimen containing a (110) Si wafer oxidized as described above. The SiO_2 layer appears in dark contrast and the light gray areas are the underlying Si substrate. The regularly arranged, aligned horizontal nanochannels appear as bright spots in the SiO_2 layer. Their distance of 270 nm corresponds to the period imposed by LIL, whereas their cross-sectional areas are apparently uniform. Figure 2c shows a single nanochannel at higher magnification. It exhibits a triangular cross section with an edge length of 26 nm. One of the edges is parallel to the former surface of the wafer.

Oxidative self-sealing of grooves located on various types of Si wafers yields arrays of horizontal nanochannels on the wafer-scale with walls consisting of silica. For example, we

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adapted the procedure described above to (100)-oriented silicon-on-insulator (SOI) wafers containing an intermediate 250 nm thick SiO_2 layer ("insulator") covered by a 500 nm thick Si layer (SOI layer) and an uppermost 50 nm thick SiO_2 layer (see the Supporting Information). Potential applications for such structures include their use as components in nanofluidic devices and the investigation of the mobility and internal dynamics of biomolecules in one-dimensional confinement by means of single molecule spectroscopy.[24] Moreover, we assume that oxidative self-sealing may be adapted to other types of patterns. For example, the self-sealing of cylindrical pores should result in the formation of closed cavities.

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Supporting Information Available: Figures S1 and S2, oxidative self-sealing of grooves in a (100)-oriented SOI wafer; Figure S3, channels obtained by oxidative self-sealing widened by wet-chemical etching. This material is available free of charge via the Internet at http://pubs.acs.org.

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